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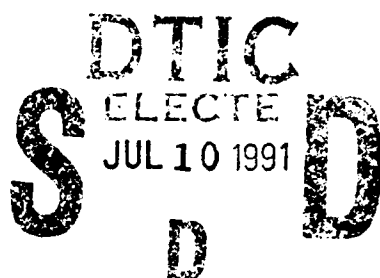
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FINAL REPORT:

ONR Contract #N00014-87-K-0780

DESIGN AND HARDWARE IMPLEMENTATION OF NEURAL SYSTEMS

Principal Investigator : Paul Mueller

Project Period: 10/01/87 - 9/30/88

SUMMARY:

This project had two major aims. One was is the design and computer simulation of specific neural circuits modeled after the early vision system of higher vertebrates. The second aim was the design and construction of electronic analog neural systems that could be used for implementing such a vision system and possibly other neural systems. Our initial approach to the hardware implementation was to build an entirely hardwired system using VLSI assemblies of electronic neurons and separate resistive synapse connection matrices fabricated by CVD deposition of amorphous silicon. During further simulation studies of the vision system it became clear that at this early state of development a completely hardwired system would be too restrictive and for this reason we felt that we needed a system that would incorporate modifiable synapses and a programmable connection architecture. Rather than restrict the design of such a system by tailoring it to the specific architectures of the vision system, we decided to design a general purpose programmable neural analog computer that would be useful not only for vision but also for other task of real world computation and other problems suitable for neural computation.

DETAILED REPORT:

Simulations of a Neural Vision System

The vision system simulations implemented in a simplified manner the basic functions of a retina and the primary visual cortex as far as they are concerned with the

decomposition of static images into visual primitives such as oriented edges and lines of different spatial scales and contrast sign as well as their end points and curvature. The system consisted of many layers of neurons each layer tuned to specific primitive (for a more detailed description see reference 10. Initial simulations were performed on systems that had only feed-forward connections from a receptor array to arrays of ON CENTER and OFF CENTER units and from there to orientation arrays. During further work it became clear that certain problems such as the disambiguation of contrast direction for oriented edges required mutually inhibitory connections between units in different arrays and that the simulation of such connections by digital methods would be prohibitively time consuming even on a supercomputer.

Our inability to explore the synaptic gains and architectures for these inhibitory connections as well as the difficulty of determining an optimal architecture and connectivity through simulation were some of the reasons for considering a programmable analog network. Another reason came from difficulties in manufacturing precise resistive networks with available technology. We manufactured several runs of resistive arrays in collaboration with Solarex Co. and found that we could not manufacture resistors of the needed high values with better than $\pm 20\%$ accuracy. Testing our vision system at this level of accuracy of the synaptic weights in extensive simulations, we found that results were marginal and that we would either have to spend considerable effort in trying to achieve better resistance tolerances or to develop programmable synapses that would allow us to tune each synapse individually and would provide us with means for rapidly exploring different connectivities. These reasons as well as our growing appreciation for the need of a programmable machine led us to direct our hardware efforts towards the design and implementation of a general purpose neural machine.

General Purpose Neural Analog Computer

The following is a brief description of the design. The architecture of the machine is loosely based on the cortex of higher vertebrates, in the sense that there are sets of individual neurons each of which receives only a limited number of inputs, that is not every neuron is connected to every other neuron. However in contrast to biological systems, our machine would be able to modify the connection architecture by external control and thus allow exploration of different architectures in addition to adjustment of synaptic weights and neuron parameters. Although the connections and synaptic gains are under digital control the machine runs in analog mode. A modular design allows expansion to any degree and at moderate to large size, i.e. 10^3 to 10^6 neurons, operational speed and power would exceed any currently available digital computer.

The machine contains large numbers of the following separate elements: **neurons, synapses, routing switches, and connection lines**. Arrays of these elements are fabricated on VLSI chips which are mounted on planar leadless chip carriers each of which forms a

separate module. These modules are connected directly to neighboring modules. By increasing the number of modules the machine can be expanded to any degree. All parameters such as the connections between different neuron groups, individual synaptic gains and neuron parameters, (threshold and time constant) are set digitally from separate microprocessor. In addition to the analog outputs from the neurons which feed into the other neurons, the neural outputs are also multiplexed, A-D converted and fed into a digital computer that uses this information in a learning mode to set connections and synaptic weights.

The neuron design is based on an earlier version which we have used in a neural machine for acoustical pattern recognition. We have designed and fabricated a VLSI test chip and have evaluated its performance which agreed with our specifications. A modified version of the design which is tailored for the large network, uses less area and has only one input, is currently at the foundry. The synaptic modules contain arrays of synapses. The synaptic gain or weight of each synapse is set from the microprocessors by serial digital inputs which are stored at each synapse. Dynamic range of the gain covers the range from 0 to 10 with a logarithmic 5 bit resolution, a 6th bit determines the sign. Implementation of the weights is by current mirrors; however, other methods are also being considered.

The switch modules serve to route the signals between the neurons and thus determine the connectivity. Each module contains a cross-point array of analog switches which are set by serial digital input. There is also a set of serial switches that can disconnect selected input and output lines. The line modules contain fixed lines that serve as fillers between the switch modules.

All chips are mounted on identical leadless planar chip carriers. Input and output lines of the carriers are arranged at right angles, with identical leads on opposite sides. Groups of chip carriers are mounted on special boards and connected to each other by elastomeric anisotropic connectors (so called zebra strips).

For real-world pattern analysis, input to the computer can be generated either by special transducer arrays such as an electronic retina, cochlea or tactile sensors, for other computational tasks, input is provided by the central digital computer through activation of selected neuron populations. This is achieved by shifting their thresholds into the negative region. Selected outputs are available either analog from the routing switches, or in digital form after multiplexing and A/D conversion.

Connections, synaptic gains and time constants are set by the central computer either from stored program libraries that contain connection architecture and synaptic constants appropriate for specific tasks or from connection parameters which are computed from neuron outputs on the basis of various learning algorithm. Special routing routines track already occupied lines, switches and synapses and adjust connection pathways accordingly.

Publications:

Mueller,P., Blackman,D., Spiro,P. and Furman,R.E., Neural Computation of visual images, Biophysical Journal, 51,441 a 1987.

Mueller,P. Neural Computation of Pattern Primitives. AIP Conference on Neural Networks for Computing, Snowbird, Utah, 1988.

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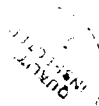
Mueller,P., Hopfield,J., Lau,C. Mead, C., Report on a Workshop "Hardware Implementation of Neuron Nets and Synapses". IEEE Circuits and Devices Magazine, 4(3) : 23 -24, 1988.
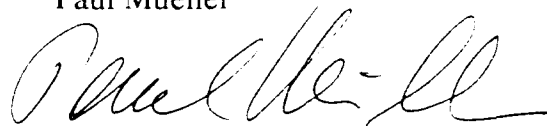
Paul Mueller

Principal Investigator

Final Patent Report on ONR Contract N00014-87-J-0780

"Design and Hardware Implementation of Neural Systems"

Principal Investigator: Paul Mueller

No Patents have been issued or were applied for.

Paul Mueller

Principal Investigator